

Vlsi Modeling Of High Speed Dedicated Short Range Communication Application Systems

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Abstract

To promote intelligent and smart transportation services into our daily life the dedicated short range communication is an advanced technique. Data encoding techniques like FM0 and Manchester encoders are used to promote communication among vehicles. These encoding techniques generally works at transistor level hence the transmitted signal reach with dc-balance, enhance the signal reliability. In existing works the design has the limitation that it does not support fully reused VLSI architectures. To rectify these problems, the FM0 and Manchester encoders are designed with SOLS technique to achieve high speed and fully reused VLSI architectures for DSRC application systems. The performance of this paper is implemented on post layout simulation in 45nm CMOS technology. This model not only supports fully reused architecture but also provides high performance.

I. INTRODUCTION:

Now-a-days the use of automobiles for transportation has become crucial into our daily life, at the same time people face several problems due to traffic grids, accidents and vehicle damages. The DSRC is the only solution to promote smart transportation services. The DSRC can be classified into two types. They are automobile-to-automobile and automobile-to-roadside. In automobile-to-automobile, the DSRC has the ability of message sending and broadcasting among vehicles for safety issues and public information announcement. The safety messages include blind-spot, intersection warning, inter-cars distance and collision-alarm. The automobile-to-roadside concentrate on smart transportation service such as electronic toll collection system. ETC can be expanded to the payment for parking-service, and gas-refueling. Thus DSRC plays a vital role in latest automobile industry. The system architecture of DSRC transceiver is shown in Fig1. consists of three primary modules namely microprocessor, base band processing and RF front-end.

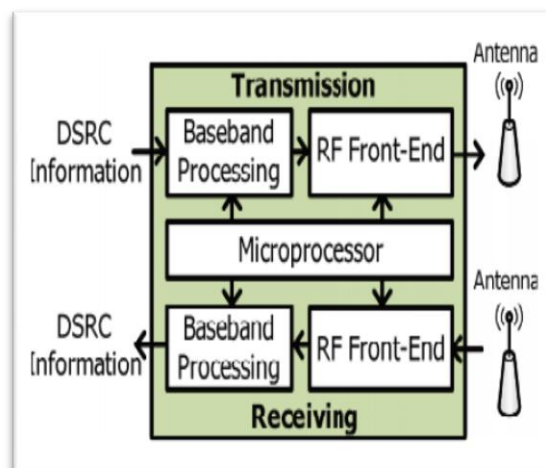


Fig1. DSRC transceiver

A Generally in communication system the transmitted signal consists of binary sequence, difficult to obtain dc-balance. Different modulation techniques like amplitude shift keying, phase shift keying and orthogonal frequency division multiplexing and encoding techniques like FM0 and Manchester codes are introduced to get the transmitted signal with dc-balance. The FM0 and Manchester codes are mostly adopted for downlink. The remainder of this paper is organized as follows. Section II describes the related work. Section III describes the coding principles of FM0 and Manchester codes. Section IV gives a hardware analysis of FM0 and Manchester encoders. In section V the VLSI architecture design using SOLS

technique is reported. The experiment results and discussion are presented in section VI. Finally, the conclusion is given in section VII.

II. RELATEDWORK:

The literature [4] targets a VLSI architecture of Manchester encoder for optical communications, implemented by 0.35- μm CMOS technology and its operation frequency is 1 GHz. The literature [5] further replaces the architecture of switch in [4] by the nMOS device. It is realized in 90-nm, CMOS technology, and the maximum operation frequency is as high as 5 GHz. The literature [6] develops a high-speed VLSI architecture almost fully reused with Manchester and Miller encodings for RFID applications. This design is realized in 0.35- μm CMOS technology and the maximum operation frequency is 200 MHz. The literature [7] also proposes a Manchester encoding architecture for ultra high frequency (UHF) RFID tag emulator, realized into FPGA prototyping system, maximum operation frequency of this design is about 256 MHz. The similar design methodology is further applied to individually construct FM0 and Miller encoders also for UHF RFID Tag emulator [8]. Its maximum operation frequency is about 192 MHz. Furthermore, [9] combines frequency shift keying (FSK) modulation and demodulation with Manchester code in hardware implementation.

III. CODING PRINCIPLES OF FM0 AND MANCHESTER CODE:

In this section, the clock signal and the input data are noted as CLK and X. with this parameters the coding principles of FM0 and Manchester codes are explained as follows.

A. FM0 Encoding

As shown in Fig.2, for each X, the FM0 code consists of two parts: one for former-half cycle of CLK, A, and the other one for later-half cycle of CLK, B.

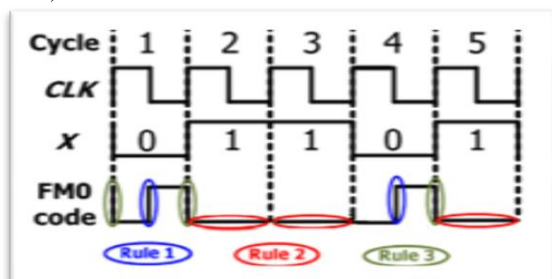


Fig 2. FM0 Encoding

The coding principle of FM0 is listed as the following three rules.

- 1) If X is the logic-0, the FM0 code must exhibit a transition between A and B.
- 2) If X is the logic-1, no transition is allowed between A and B.
- 3) The transition is allocated among each FM0 code no matter what the X is.

B. Manchester Encoding

The Manchester coding example is shown in Fig. 3. The Manchester code is derived from $X \oplus \text{CLK}$. The Manchester encoding is realized with a XOR operation for CLK and X.

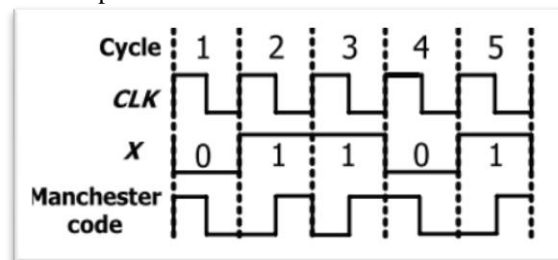


Fig 3. Manchester Encoding

IV. HARDWARE ARCHITECTURE OF FM0 AND MANCHESTER ENCODERS

The hardware architectures of FM0 and Manchester encoders are shown in Fig.4.

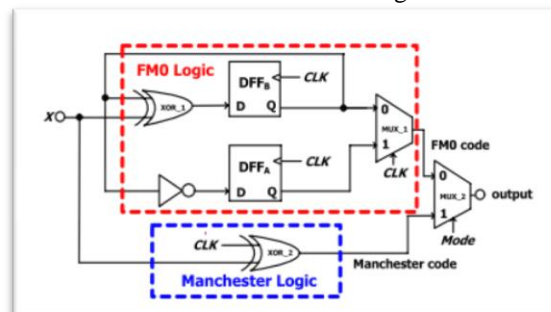


Fig 4. Architecture of FM0 and Manchester encoder

The upper part is for FM0 encoder and bottom part is the architecture of Manchester encoder. To measure hardware utilization, the hardware utilization rate (HUR) is calculated as

$$\text{HUR} = \frac{\text{Active components}}{\text{Total components}} \times 100\%.$$

The active components mean the components that work for FM0 or Manchester encoding. The total components are the number of components in the entire hardware architecture. For FM0 encoding, the active components are 6, and its HUR is 85.71%. For Manchester encoding, the active components are 2, comprising XOR – 2 and MUX – 2, and its HUR is as low as 28.57%. On average, this hardware architecture has a poor HUR of 57.14%, and almost

half of total components are wasted. The transistor count of the hardware architecture without SOLS technique is 98, where 86 transistors are for FM0 encoding and 26 transistors are for Manchester coding. On average, only 56 transistors can be reused.

V. DESIGN OF FM0 AND MANCHESTER ENCODER USING SOLS TECHNIQUE

The need for SOLS technique is to design a fully reused VLSI architecture for FM0 and Manchester codes. SOLS technique is having two core concepts: area-compact retiming and balance logic operation sharing.

A. Area-Compact Retiming

Illustration of area-compact retiming on FM0 encoding technique is shown in Fig 5.

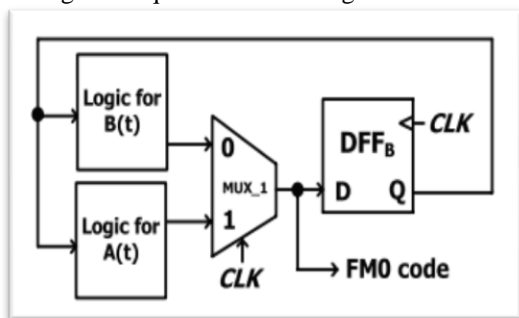


Fig5. FM0 encoding with area compact retiming

For FM0, the state code of each state is stored into DFFA and DFFB. But the architecture requires a single 1 bit flip-flop to store the states. Removal of DFFA causes the logic fault of FM0 code due to non-synchronization between A(t) and B(t). DFFB is relocated after mux_1 to avoid logic faults. The transistor count of the FM0 encoding architecture without area-compact retiming is 72, and that with area-compact retiming is 50. The area-compact retiming technique reduces 22 transistors. Thus the area-compact retiming relocates the hardware resource to reduce 22 transistors.

B. Balance Logic-Operation Sharing

The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. It is illustrated in the Fig 6.

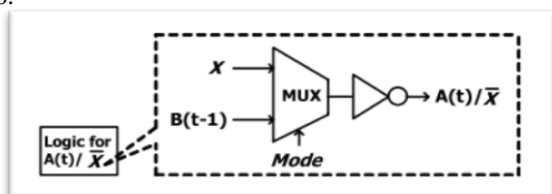


Fig 6. Balance Logic operation sharing

The concept of balance logic-operation sharing is to integrate the X into A(t) and X into B(t), respectively. The logic for A(t)/X is shown in Fig.6. The A(t) can be derived from an inverter of B(t-1), and X is obtained by an inverter of X. The logic for A(t)/X can share the same inverter, and then a multiplexer is placed before the inverter to switch the operands of B(t-1) and X. The Mode indicates either FM0 or Manchester encoding is adopted. By analyzing the two core concepts of SOLS technique the VLSI architecture of FM0 and Manchester encoding is shown in Fig 7.

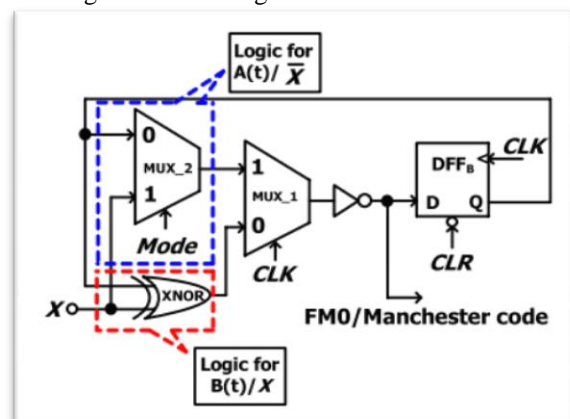


Fig7. VLSI Architecture using SOLS Technique

The SOLS technique improves the HUR from 57.14% to 100%, whether the FM0 or Manchester code is adopted. Thus, the SOLS technique provides a fully reused VLSI architecture for FM0 and Manchester encodings with the HUR of 100%. The logic functions of SOLS technique can be realized by various logic functions to optimize more performance such as area, power, speed. The proposed SOLS technique is developed from the architecture perspective to achieve 100% HUR. If the logic components in SOLS architecture are designed using static CMOS, the Manchester delay is seriously limited owing to too many transistors in the critical path of Manchester encoder. To further reduce the transistor count in Manchester encoding path, the transmission-gate logic is considered in the circuit designs of MUX-1, MUX-2 and XNOR. The propagation delay of transmission-gate logic is less than that of static CMOS. Applying the transmission gate logic can compact the transistor count to reduce the propagation delay.

VI. EXPERIMENT RESULTS AND DISCUSSION

This paper is compared with the previous articles which are implemented in two kinds of design flows. The literatures [4] and [5] are realized with full-

custom and the literatures [7]–[9] are designed with FPGA. The design flow of the full-custom is Microwind3.1 of 45nm 1P6M CMOS technology, and the Xilinx development board is adopted for the FPGA design-flow. The performance of full-custom design flow is from post-layout simulation. The CMOS technologies of these works include 0.35μm, 90 nm, which are not identical to 0.18μm adopted in this paper. Our work targets at an efficient integration of hardware devices for Manchester encoding and FMO encoding instead of operation frequency and power consumption. Generally, more coding methods a hardware architecture can support, more hardware devices it requires. Table I shows the implementation result of FMO and Manchester logics. The evaluation platform consists of two coding methods, and how to efficiently allocate hardware devices to perform them is a critical design issue for performance evaluation. To measure the device-efficiency of each work, two figure of merits (FOMs) are defined as follows:

$$\begin{cases} \text{FOM}_1 = \frac{\text{Data rate}}{\text{Total devices}} & ; (\text{Mb/s/device}) \\ \text{FOM}_2 = \frac{\text{Total devices}}{\text{Total coding modes}} & ; (\text{device/coding mode}) \end{cases}$$

where the data rate is either for FMO or Manchester encoding. Total coding modes denote how many coding methods a hardware architecture can support. In this evaluation platform, total coding modes are set to 2, representing FMO and Manchester encodings. The total devices mean the total transistor count and total FPGA resource for full-custom and FPGA designs, respectively. FPGA resource incorporates Slice, Flop-Flip, LUTs, and Bonded IOBs.

Table I Implementation results of FMO and Manchester logics.

	Previous work	Previous work	Present work
Realization	180nm CMOS	Xilinx spartan2	Xilinx spartan3E,4 5nm CMOS
Supply voltage	1.8 V	3.3 V	2.5 V, 1.80 V
Combination of article	[4]-[5]	[7]-[9]	proposed
HUR	57.14 %	57.14%	100%
FPGA resource usage	N/A	Slice: 1 Flip flop: 1 LUTs: 1 Bonded IOBs:5	Slice: 1 LUTs: 2 Bonded IOBs:4

This paper is also implemented with FPGA not only for an objective comparison but also for the functional prototyping. The waveforms of the functional verification are shown in Fig. 8, where the FMO and Manchester encodings are shown in Fig. 8(a) and 8(b), respectively.

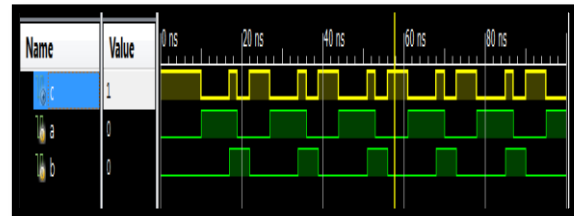


Fig 8(a). FMO Encoding

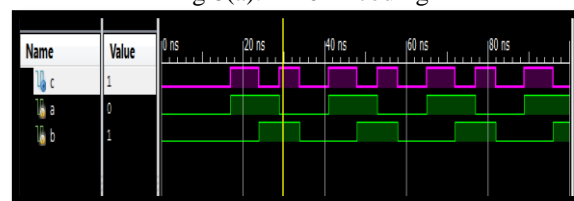


Fig 8(b). Manchester Encoding

The RTL and Technology Schematic of both the FMO and Manchester encoding techniques are shown in Fig 9. and Fig 10. Respectively. The timing summary shows that the delay factor for Manchester and FMO encoders is 5.776 ns.

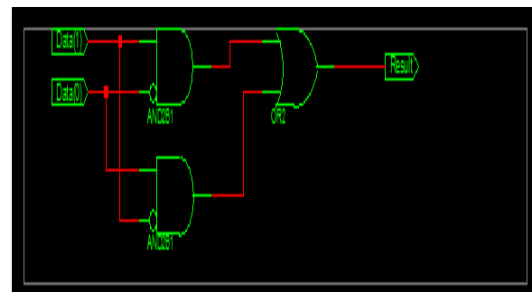


Fig 9. RTL Schematic

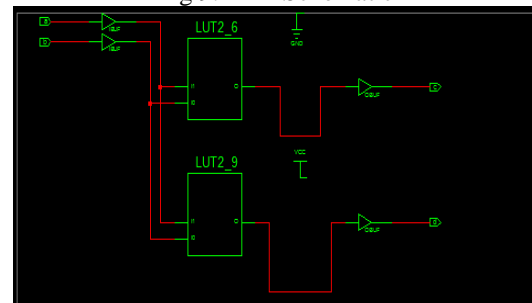


Fig10 Technology Schematic

The layout view of FMO and Manchester encoders are shown in Fig 11. and Fig 12. Layouts are implemented in 90nm CMOS technology the power consumption for FMO encoder is 1.43mW. and for Manchester logic the power consumption is about 1.70mW.

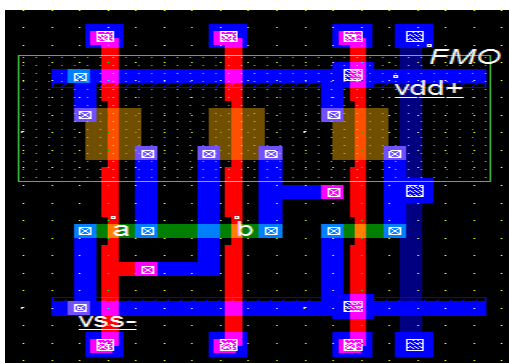


Fig 11. Layout of FMO Encoder

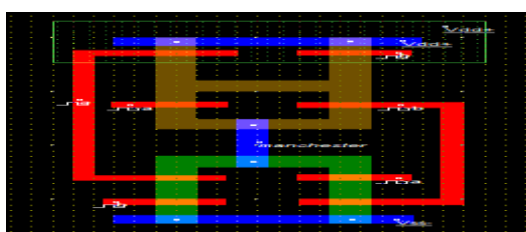


Fig12. Layout of Manchester Encoder

VII. CONCLUSION

In this paper, the completely reused VLSI structural engineering utilizing SOLS strategy for both FMO and Manchester encodings will be proposed. This paper is acknowledged in 45nm CMOS innovation with extraordinary gadget proficiency and implemented by using Microwind3.1 for post layout synthesis. The timing analysis are verified on Xilinx simulator. The Xilinx9.2i software is utilized in the project and code is written on Verilog HDL. The target FPGA prototyping device is belongs to Spartan3E family and the device is XC3S100E which has speed grade of -5. The power consumption is 1.48mW and the delay is 5.776ns. The SOLS technique gives high performance when compared to existing articles. In future the design may implemented using high performance FPGA devices and the Nanometer may be reduced from 45nm to 32 nm CMOS technology.

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REFERENCES

- [1] F. Ahmed-Zaid, F. Bai, S. Bai, C. Basnayake, B. Bellur, S. Brovold, et al., Rep. DOT HS 810 591, Sep. 2011.
- [2] J. B. Kenney, "Dedicated short-range communications (DSRC) standards in the United

States," Proc. IEEE, vol. 99, no. 7, pp. 1162–1182, Jul. 2011.

- [3] J. Daniel, V. Taliwal, A. Meier, W. Holfelder, and R. Herrtwich, Mag., vol. 13, no. 5, pp. 36–43, Oct. 2006
- [4] P. Benabes, A. Gauthier, and J. Oksman, Proc. IEEE, Int. Conf. Electron., Circuits Syst., vol. 3, Dec. 2003, pp. 1156–1159.
- [5] A. Karagounis, A. Polyzos, B. Kotsos, and N. Assimakis, Proc. 16th Int. Conf. Syst., Signals Image Process., Jun. 2009, pp. 1–4.
- [6] Y.C Hung , High speed CMOS chip design for Manchester and miller encoder, proc Intell.inf hiding multimedia signal process.,sep.2009,pp. 538-541.
- [7] M. A. Khan, M. Sharma, and P. R. Brahmanandha, "FSM based Manchester encoder for UHF RFID tag emulator," inProc. Int. Conf. Comput., Commun. Netw., Dec. 2008, pp. 1–6.
- [8] M. A. Khan, M. Sharma, and P. R. Brahmanandha, "FSM based FMO and Miller encoder for UHF RFID tag emulator," inProc. IEEE Adv. Comput. Conf., Mar. 2009, pp. 1317–1322.
- [9] J.-H. Deng, F.-C. Hsiao, and Y.-H. Lin, "Top down design of joint MODEM and CODEC detection schemes for DSRC coded-FSK systems over high mobility fading channels," inProc. Adv. Commun. Technol. Jan. 2013, pp. 98–103

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